UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/570,290	02/28/2006	Adrianus Josephus Bink	NL031031	5446

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ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
10/30/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>23 July 2009</u>.
2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-20</u> is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) <u>1-20</u> is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a) ☐ All   b) ☐ Some * c) ☐ None of:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

In view of the appeal brief filed on 7/23/2009, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

The instant application having Application No. 10/570,290 has a total of 20 claims pending in the application, there are 2 independent claims and 18 dependent claims, all of which are ready for examination by the examiner.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, 5, 7-11, 14, 15, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emma et al (US 5,584,002) in view of Lasserre et al (US 2002/0065988).

Regarding Claim 1, Emma teaches an integrated circuit, comprising:

at least one processing unit **(Processor 340 in Figure 5)**;

a cache memory having a plurality of memory modules for caching data **(Cache Unit 300 in Figure 5, with modules corresponding to the entries storing data 314 and 316 in Figure 5)**, wherein the cache memory comprises a plurality of distinct physical banks, wherein each physical bank comprises some of the memory modules **(each bank corresponds to a congruence class in Emma, Column 1 Lines 38-41, and the congruence class is a physical bank, as the congruence classes are described as a row with "a single set or location within the row into which a given datum may be stored", Column 1 Lines 61-63, and the embodiment of Figure 5 shows congruence classes with two sets [Column 8 Lines 27-29] along with gates and flip flops, indicating that it is a physical block diagram and not logical)**;

remapping means for performing an unrestricted remapping within said plurality of memory modules **(inherently present to remap the data from one congruence class to another congruence class, Column 3 Lines 54-58)**, wherein the unrestricted remapping permits remapping the memory modules from a first physical bank of memory modules to a second physical bank of memory modules **(Column 3 Lines 54-**

58, when the data is remapped from a first congruence class to a second

congruence class, it is going from a first bank to a second bank).

However, Emma does not teach wherein each physical bank is configured to

facilitate serving a read/write request independently of other physical banks to allow

concurrent transfers for at least two of the physical banks.

Lasserre teaches a cache configured into distinct portions, and "requests in each

portion can be serviced concurrently" **(Paragraph 0007 in Lasserre)**.

It would have been obvious to a person having ordinary skill in the art at the time

the invention was made to which the subject matter pertains to have implemented the

congruence classes of Emma as the portions of Lasserre, thereby facilitating service of

read/write requests independently of other portions to allow concurrent transfers for at

least two of the physical banks, because allowing concurrent accesses means no

processor will have to wait for data, thereby improving performance. Thus, by

combining the devices, additional benefits are obtained.

Regarding Claim 2, Emma and Lasserre teach the integrated circuit according

to Claim 1, and Emma further teaches wherein said cache memory is a set-associative

cache (Column 8 Lines 20-22).

Regarding Claim 4, Emma and Lasserre teach the integrated circuit according

to Claim 1, and Emma further teaches wherein said remapping means is adapted to

perform the remapping on the basis of a reduction mapping, wherein the reduction

mapping performs the remapping using less output symbols than input symbols

(Column 9 Lines 5-18, where the remapping means must take as input the congruence

and synonym class parameters but only output the identification (AMID) bits, therefore

there are fewer output symbols than input symbols).

Regarding Claim 5, Emma and Lasserre teach all limitations of Claim 1, and

Emma further teaches:

a Tag RAM unit associated to said cache for identifying which data is cached in

said cache memory (included in Cache Directory 310 of Figure 5, the AHIGH field 307

acts as a tag);

wherein said remapping means is arranged in series with said Tag RAM unit

(Column 9 Lines 5-18, since the remapping is done at power-on, the remapping is done

prior to any checking of the Tag RAM, thus the remapping and Tag RAM are arranged

serially).

Regarding Claim 7, Emma and Lasserre teach all limitations of Claim 5, and

Emma further teaches a look up table for marking faulty memory modules (Column 9

Lines 9-11, the SC bit of each cache entry acts as a look up table for each faulty

module).

Regarding Claim 9, Emma and Lasserre teach all limitations of Claim 1, and

Emma further teaches wherein the remapping means is further configured to distribute

faulty memory modules evenly over a plurality of banks (Column 9 Lines 5-18, where

alternate congruence classes are selected among synonym classes, thus a fault in a

particular bank is mapped to a particular synonym class, and a fault from a different

bank would be mapped to a different synonym class, thereby evenly distributing the

faults, also see how each congruence class is assigned a synonym class, Column 3

Lines 26-35).

Regarding Claim 10, Emma and Lasserre teach all limitations of Claim 1, and

Emma further teaches wherein the remapping means is further configured to perform an

unrestricted remapping at a block/line granularity level of modules (Emma teaches

remapping at a line granularity, Column 3 Lines 33-35).

Regarding Claim 11, Emma and Lasserre teach the integrated circuit according

to Claim 1, and Emma further teaches wherein the remapping means is further

configured to remap at least one of the memory modules from an index to a different

index (Column 5 Lines 5-18, the remapping is done by remapping the AMID field

[corresponding to the cache index] in a different congruence class).

Regarding Claim 15, Emma and Lasserre teach all limitations of Claim 5, and

Emma further teaches a look up table for marking faulty memory modules (Column 9

Lines 9-11, the SC bit of each cache entry acts as a look up table for each faulty

module).

Regarding Claim 8, Emma teaches a method of cache remapping in an

integrated circuit having at least one processing unit **(Processor 340 in Figure 5)**; a

main memory for storing data **(present between the cache and processor, Column 2**

Lines 42-44); and a cache memory having a plurality of memory modules for caching

data **(Cache Unit 300 in Figure 5, with modules corresponding to the entries**

storing data 314 and 316 in Figure 5), the method comprising:

performing an unrestricted remapping within said plurality of memory modules

(Column 3 Lines 54-58, when the data is remapped from a first congruence class

to a second congruence class), wherein the memory modules are distributed among

a plurality of distinct physical banks within the cache memory **(each bank corresponds**

to a congruence class in Emma, Column 1 Lines 38-41, and the congruence class

is a physical bank, as the congruence classes are described as a row with "a

single set or location within the row into which a given datum may be stored",

Column 1 Lines 61-63, and the embodiment of Figure 5 shows congruence

classes with two sets [Column 8 Lines 27-29] along with gates and flip flops,

indicating that it is a physical block diagram and not logical), wherein the

unrestricted remapping permits remapping the memory modules from a first bank of

memory modules to a second bank of memory modules **(Column 3 Lines 54-58, when**

the data is remapped from a first congruence class to a second congruence

class, it is going from a first bank to a second bank).

However, Emma does not teach wherein each physical bank is configured to

facilitate serving a read/write request independently of other physical banks to allow

concurrent transfers for at least two of the physical banks.

Lasserre teaches a cache configured into distinct portions, and "requests in each

portion can be serviced concurrently" **(Paragraph 0007 in Lasserre)**.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the congruence classes of Emma as the portions of Lasserre, thereby facilitating service of read/write requests independently of other portions to allow concurrent transfers for at least two of the physical banks, because allowing concurrent accesses means no processor will have to wait for data, thereby improving performance. Thus, by combining the devices, additional benefits are obtained.

Regarding Claim 14, Emma and Lasserre teach the integrated circuit according to Claim 8, and Emma further teaches wherein said remapping means is adapted to perform the remapping on the basis of a reduction mapping, wherein the reduction mapping performs the remapping using less output symbols than input symbols (Column 9 Lines 5-18, where the remapping means must take as input the congruence and synonym class parameters but only output the identification (AMID) bits, therefore there are fewer output symbols than input symbols).

Regarding Claim 18, Emma and Lasserre teach all limitations of Claim 8, and Emma further teaches the remapping means is further configured to remap at least one of the memory modules to a new way and a same index within the second physical bank of memory modules (Column 5 Lines 5-18, the remapping is done by remapping the AMID field [corresponding to the cache index] in a different congruence class).

Claims 3, 13, and 17 are rejected under U.S.C. 103(a) as being unpatentable over Emma and Lasserre in further view of Asher (US 6,671,822).

Regarding Claim 3, Emma and Lasserre teach all limitations of Claim 1 as described above. However, Emma does not teach a programmable permutation means for remapping. Asher teaches remapping means adapted to perform the remapping on the basis of a programmable permutation function (see bus 18 in Figure 2, which uses a multiplexer to permute way 0 to another given way; it is the multiplexer select bits that enable this permutation mapping to be programmed). It would have been obvious to a person of ordinary skill in the art to which the subject matter pertains at the time the invention was made to have used programmable permutation functions instead of a reduction mapping, since programmable permutation functions allow for greater flexibility in choosing which line to remap to (Column 6 Lines 21-22 in Asher).

Regarding Claim 13, Emma and Lasserre teach the circuit according to Claim 1, but do not teach wherein the remapping means is further configured to remap at least one of the memory modules to a new way and a same index within the second physical bank of memory modules.

Asher teaches remapping a cache, where the device is configured to remap a memory module to a new way and a same index within a different bank of memory modules (Column 6 Lines 41-59 in Asher).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have allowed the device of Emma to remap to a new way and same index to allow more flexibility. Thus, by combining the devices, additional benefits are obtained.

Regarding Claim 17, Emma and Lasserre teach the circuit according to Claim 1, but do not teach wherein the remapping means is further configured to remap at least one of the memory modules to a new way and a same index within the second physical bank of memory modules.

Asher teaches remapping a cache, where the device is configured to remap a memory module to a new way and a same index within a different bank of memory modules (Column 6 Lines 41-59 in Asher).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have allowed the device of Emma to remap to a new way and same index to allow more flexibility. Thus, by combining the devices, additional benefits are obtained.

Claim 6 is rejected under U.S.C. 103(a) as being unpatentable over Emma and Lasserre in further view of Kramer (US 4,868,869).

Regarding Claim 6, Emma and Lasserre teach all limitations of Claim 1 as been discussed above. However, Emma does not teach a Tag RAM in parallel with said remapping means. Kramer teaches several lookup tables and additional circuitry (which is what a Tag RAM unit and a remapping unit with Map RAM are) connected in parallel (see Figure 9 in Kramer). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains to have placed the Tag RAM and remapping means of Emma in parallel as taught by

Kramer. As motivation, connecting circuitry in parallel generally leads to a faster circuit.

Thus, by putting the units in parallel, additional benefits are obtained.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Emma

and Lasserre in view of the Examiner's taking of Official Notice.

Regarding Claim 12, Emma and Lasserre teach the circuit according to Claim 1,

but are silent on what the cache memory comprises.

However, it is well known in the art to use DRAM for modules for a cache

memory.

It would have been obvious to a person having ordinary skill in the art at the time

the invention was made to which the subject matter pertains to modify the combination

of Emma and Lassere to implement DRAM for the caching modules, since DRAM costs

less than many other memory chips.

Regarding Claim 16, Emma and Lasserre teach the circuit according to Claim 8,

but are silent on what the cache memory comprises.

However, it is well known in the art to use DRAM for modules for a cache

memory.

It would have been obvious to a person having ordinary skill in the art at the time

the invention was made to which the subject matter pertains to modify the combination

of Emma and Lassere to implement DRAM for the caching modules, since DRAM costs

less than many other memory chips.

Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emma and Lasserre in view of Swenson (US 5,519,846).

Regarding Claim 19, Emma and Lasserre teach the circuit according to Claim 1, but do not teach wherein each physical bank of memory modules is located on a separate DRAM module.

Swenson teaches a cache storage that includes multiple DRAM storage modules (Column 4 Lines 58-59).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have implemented separate DRAM modules for multiple banks in the device of Emma and Lassere, because allowing multiple DRAM modules in the cache allows for greater flexibility in adding capacity to the cache.

Regarding Claim 20, Emma and Lasserre teach the circuit according to Claim 8, but do not teach wherein each physical bank of memory modules is located on a separate DRAM module.

Swenson teaches a cache storage that includes multiple DRAM storage modules (Column 4 Lines 58-59).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have implemented separate DRAM modules for multiple banks in the device of Emma and Lassere, because allowing multiple DRAM modules in the cache allows for greater flexibility in adding capacity to the cache.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

Rejections - USC 102/103

Applicant's arguments in the Appeal Brief filed 7/23/2009 are persuasive and, therefore, the finality of the previous action is withdrawn. However, a new rejection has been made in light of a newly found prior art reference.

CLOSING COMMENTS

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-20 have received a first action on the merits and are subject of a first action non-final.

DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571) 270-3565 and can normally be reached on Monday - Thursday 7:30am – 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

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October 28, 2009